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EXAMINER
TRAN, KHANH C

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/634,597	Applicant(s) CUMMINGS ET AL.	
	Examiner Khanh Tran	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,11-13,15,18-24,27,29 and 31-37* is/are rejected.

7)☒ Claim(s) *2-10,14,16,17,25,26,28 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 10/07/2004. Claims 1-37 are pending in this Office action.

Response to Arguments

2. Applicant's arguments with respect to claims 1,15, 18, 27 and 31-37 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claim 5 is objected to because of the following informalities: in line 7, "a synchronous" should be changed to -- asynchronous --. Appropriate correction is required.

4. Claim 8 is objected to because of the following informalities: in line 5, "a synchronous" should be changed to -- asynchronous --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 11-13, 15, 18, 20, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman et al. U.S. 6,546,451 B1 in view of MacWilliams et al. U.S. Patent 6,112,016 and Powell U.S. Patent 5,875,338.

Regarding claim 1, in column 2, lines 30-40, figure 1 illustrates a computer system 10 including a plurality of node controllers 12 interconnected by a network 14. Each node controller processes data and traffic both internally and with other node controllers 12 within computer system 10 over network 14. Each node controller communicates with a local processor 16, a local memory device 17, and a local input/output device 18.

Venkataraman et al. does not expressly teach that local processor 16, local memory device 17, and local input/output device 18 being synchronous devices as claimed in the application claim. MacWilliams et al. discusses in Background of the Invention in another US Patent that in column 3, lines 4-30, high-speed processor chip typically interfaces with the rest of computer using one of two high-speed buses. One of the two high-speed buses is a relatively high speed synchronous bus called a local bus. High bandwidth devices such as graphics adapter cards and fast input/output (I/O) devices can be coupled directly to the synchronous local bus. In view of MacWilliams et al. discussion, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the local processor 16, I/O device 18, and local memory device 17, as

taught in Venkataraman et al. invention, are synchronous devices because local processor 16 communicates with I/O device 18, and local memory device 17 through synchronous local bus as discussed in MacWilliams et al. invention. Furthermore, as disclosed in column 3, lines 15-50 of Venkataraman et al. invention, the processor core runs faster as a multiple of its system interface bus. As appreciated by a person of average skill in the art of computer system that I/O device 18 runs slower than the processor speed and is not the same speed with the node controller 12. In light of the foregoing discussion, local processor 16 has an associated clock domain characterized by the clock speed as discussed above, I/O device 18 has an associated clock domain characterized by different clock speed as discussed above. Hence, local processor 16 and I/O device 18 correspond to the claimed plurality of synchronous modules.

In column 2 lines 40-57 of Venkataraman et al. invention, node controller 12 includes a network interface unit 20, a memory directory interface unit 22, a processor interface unit 24, an input/output interface unit 26, a local block unit 28, and a crossbar unit 30. In column 3, lines 15-30, Venkataraman et al. expresses that there may be asynchronous boundaries between processor interface unit 24 and crossbar unit 30 and between input/output interface unit 26 and crossbar unit 30. In light of the foregoing disclosure, crossbar unit 30 can operate in the asynchronous domain with local processor 16 via processor interface unit 24 or with I/O device 18 via input/output interface unit 26. Venkataraman et al. further discloses that asynchronous boundary occurs as a result of a core clock driving

crossbar unit 30 being at a different non-integer ratio clock speed than the clock speed of processor interface unit 24 and its associated processor 16 or input/output interface unit 26 and its associated input/output device 18. Referring to figure 3, column 2 line 59 via column 3 line 15, crossbar 30 includes arbiter 56 that determines the configuration of data path crossbar 58 in transferring data, control messages, other traffic among all queues (e.g. Input/Output input queue 44, Input/Output input queue 46, a processor interface output queue 52, a processor interface input queue 54) within crossbar unit 30 and units of node controller 12. All queues in crossbar 30 include dual FIFO buffers. As result of that crossbar 30 is operable in asynchronous mode to implement FIFO channel between any of the two recited queues, see also figure 3. The processor queues are associated with processor 16, and I/O queues are associated with I/O device 18.

Venkataraman et al. does not expressly disclose a plurality of clock domain converters as set forth in the application claim. Nevertheless, in column 3, lines 39-67, Venkataraman et al. discloses a synchronizer 60 being used at the asynchronous boundary of crossbar unit 30 and any of Input/Output input queue 44, Input/Output input queue 46, processor interface output queue 52, processor interface input queue 54. Because Venkataraman et al. teachings disclose synchronizer 60 can be used at the asynchronous boundary of crossbar unit 30 and any of Input/Output input queue 44, Input/Output input queue 46, processor interface output queue 52, processor interface input queue 54, it would

have been obvious for one of ordinary skill in the art at the time the invention was made that synchronizer 60 performs as a clock domain converter as claimed in the application claim to convert data between clock domain of synchronous processor 16 and I/O device 18 and asynchronous domain of crossbar 30. In column 3, lines 15-40, Venkataraman et al. further teaches that because of asynchronous boundaries, data entering crossbar unit 30 from either processor interface unit 24 or input/output interface unit 26 needs to be synchronized to the core clock speed of crossbar unit 30. Hence, transmission of data through asynchronous boundaries is according to an asynchronous handshake protocol as appreciated by one of ordinary skill in the art.

Venkataraman et al. does not show an integrated circuit comprising all elements as set forth in the claim. Powell discloses in figure 2 a detailed block diagram illustrating major components of the data processing system 20 of figure 1 connected to a crossbar switch according to the invention. A person of ordinary skill in the art of computer technology would recognize that the data processing system 20 shown in figure 1 is a computer desktop. In view of that, it would have been obvious for one of ordinary skill in the art to recognize that figure 2 illustrates a PC motherboard including crossbar switch 54. As known in the art, PC motherboard includes CPU, RAM, ROM, CMOS RAM, diskette controller, serial controller, disk controller, network adapter, parallel controller, display controller, DMA controller, keyboard mouse controller, and CD-ROM controller. Venkataraman et al. and Powell teachings are in the same field of endeavor.

Venkataraman et al. teachings are computer system linked together over network 14. In view of that, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Venkataraman et al. teachings can be modified to implement on the same motherboard as taught in Powell teachings. The modification is obvious since each subsystem including a node controller 12, I/O device 18, memory 17, and processor 16 is representative of a computer. The PC motherboard is an integrated circuit.

Regarding claim 11, the crossbar unit 30 in figure 3 includes an arbiter 56. In column 3, lines 10-16, the arbiter 56 determines the configuration of datapath crossbar 58 in transferring data, control messages, other traffic, and invalidation requests among all queues within crossbar unit 30 and units of node controller 12. In view of that, arbiter 56 routes data from any of queues, corresponding to the claimed input channels, to any of second number of queues, corresponding to the claimed output channels, according to routing control information. Each combination of an input queue and output queue comprises a data path. Hence, crossbar unit 30 routes data in a deterministic manner on each of the links, thereby preserves partial ordering representing routing control information. Events on different links are uncorrelated as appreciated by one of ordinary skill in the art.

Regarding claim 12, crossbar unit 30 in figure 3 is inherently operable to transfer data based on one timing assumption.

Regarding claim 13, the one timing assumption is a pulse timing assumption as appreciated by one of ordinary skill in the art because different clocks of node controller 12 are pulse clocks.

Regarding claim 15, as discussed in claim 1, the crossbar unit 30 implements a FIFO channel between any two queues through asynchronous boundaries. Because of the FIFO scheme, the asynchronous handshaking is not sensitive of any delay as claimed in the pending application.

Regarding claim 18, referring to figure 3, also in column 2 line 59 to column 3 line 16, crossbar unit 30 includes arbiter 56, which determines configuration of datapath crossbar 58 in transferring data, control messages, other traffic, and invalidation requests among all queues within crossbar unit 30 and units of node controller 12. In view of that, the claimed feature "*the asynchronous crossbar is operable to arbitrate among multiple requests corresponding to a same destination synchronous module*" is within Venkataraman et al. teachings.

Regarding claim 20, as recited in claim 1, synchronizer 60 is used at the asynchronous boundary of crossbar unit 30 and any of Input/Output input queue 44, Input/Output input queue 46, processor interface output queue 52, processor interface input queue 54. Synchronizer 60 performs function of the claimed clock converter to synchronize data entering crossbar unit 30 from either processor interface unit 24 or

input/output interface unit 26; see column 3, lines 15-30. Referring to figure 4, in order to control the foregoing data transmission to/from crossbar unit, synchronizer 60 utilizes write address latch 62, read address latch 70, a Gray code counter 64, see column 3, lines 40-67. In light of the foregoing disclosure, write address latch 62, read address latch 70, a Gray code counter 64 would perform the function of the rate throttling circuit specified in the claim. Because write address latch 62, read address latch 70, a Gray code counter 64 control data transmission from one clock frequency to a clock frequency of crossbar unit 30, one of ordinary skill in the would have recognized the interchangeability of the elements shown in Venkataraman et al. teachings for the corresponding rate throttling circuit disclosed in the specification.

Regarding claim 27, referring to figure 2, node controller 12 includes a network interface unit 20, a memory directory interface unit 22, a processor interface unit 24, an input/output interface unit 26, a local block unit 28, and a crossbar unit 30. Venkataraman et al. further expresses that processor interface unit 24 may provide a communication link with one or more local processors 16; see column 2, lines 40-57. In view of that, each node controller associated with the recited elements above can be part of a multiprocessor system. The processor 16 inherently has cache memory. The memory directory interface unit 22 is respectively coupled to a memory controller as appreciated by one of ordinary skill in the art. The input/output interface unit 26 is coupled to an I/O device as recited in claim 1.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman et al. U.S. 6,546,451 B1, MacWilliams et al. U.S. Patent 6,112,016 and Powell U.S. Patent 5,875,338 as applied to claim 18 and further in view of admitted prior art in the original disclosure.

Regarding claim 19, Venkataraman et al. teaches a crossbar unit 30 shown in figure including an arbiter 56, corresponding to the claimed arbitration circuitry. Venkataraman et al., however, does not teach arbitration circuitry comprising at least one Seitz arbiter. Admitted prior art in the original disclosure discloses implementations of Seitz arbiter and QFR circuits in C. L. Seitz, System Timing, chapter 7, pp. 218-262, Reading, Mass., Addison-Wesley, 1980, and F. U. Rosemberger, C. E. Molnar, T. J. Chaney, and T. P. Fang, Q-modules: Internally clocked delay-insensitive modules, IEEE Trans., Computers, vol. 37, no.9, pp. 1005-1018, September 1988, respectively; see column 54, line 23 via column 55, line 5, of the original disclosure. Because of known potential benefits of Seitz arbiter, one of ordinary skill in the art would have been motivated to implement Seitz arbiter, as taught by admitted prior art, into crossbar unit 30 as taught by Venkataraman et al. in figure 3. Furthermore, implementation of new intended use (e.g. Seitz arbiter) for an old product does not make a claim to that old product patentable. In re Schreiber, 44 USPQ2d (Fed. Cir. 1997).

6. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman et al. U.S. 6,546,451 B1, MacWilliams et al. U.S. Patent 6,112,016 and

Powell U.S. Patent 5,875,338 as applied to claim 20 above, and further in view of Wicki et al. U.S. Patent 5,838,684.

Regarding claim 21, Venkataraman et al. does not teach the claimed limitations "*the rate throttling circuit is operable to control transmission of the data by delaying transmission of the data in accordance with a priority associated with the specific synchronous module*". Wicki et al. teaches a plesioasynchronous and aynchronous router circuit includes a crossbar switch (see figure 4A) for connecting an arbiter selected input buffer with a particular one of the output ports, an arbiter system for choosing one of several input buffers associated with a particular one of the output ports, the router circuit shown in figure 1. As disclosed in the Summary of the Invention, column 2 lines 5-20, Wicki et al. teaches that the router system establishes interconnection of input buffers selected by arbitration with a predetermined output port through a crossbar switch. Each output port has a dedicated arbiter to select a highest priority input buffer for connection to its output port. Furthermore, frame words are streamed independently through selected input buffers and output ports through crossbar switch. Venkataraman et al. and Wicki et al. teachings are in the same field of endeavor. Wicki et al. invention differs from Venkataraman et al. invention in that the router system establishes interconnection of input buffers selected by arbitration with a predetermined output port through a crossbar switch based on selection of highest priority input buffer for connection to its output port. In view of that, it would have been obvious for one of ordinary skill in the art at the time the

invention was made that Venkataraman et al. node controller can be modified to implement Wicki et al. teachings in accordance with a priority scheme. The modification is obvious to a person of average skill in the art that without priority scheme, as suggested by Wicki et al. teachings in column 1, lines 55-67, the crossbar unit as taught by Venkataraman et al. is hampered by congestion at crossbar output ports caused by complexity in arbitration of access to particular output ports from selected input buffers. With the combining teachings, write address latch 62, read address latch 70, a Gray code counter 64 of the synchronizer 60 control transmission of data by delaying transmission of the data in accordance with a priority associated with the specific synchronous device as appreciated by one of ordinary skill in the art.

Regarding claim 22, using analogous argument as in claim 21, with the combining teachings of Venkataraman et al. and Wicki et al., write address latch 62, read address latch 70, a Gray code counter 64 of the synchronizer 60 control transmission of data by delaying transmission of the data in response to congestion between synchronizer 60 and crossbar unit 30 as appreciated by one of ordinary skill in the art.

Regarding claim 23, as recited in claim 1, because the asynchronous boundary of crossbar unit 30 and any of Input/Output input queue 44, Input/Output input queue 46, processor interface output queue 52, processor interface input queue 54, write

address latch 62, read address latch 70, a Gray code counter 64 of the synchronizer 60 is operable to determine the congestion with reference to the asynchronous handshake protocol between the corresponding synchronizer 60 and crossbar unit 30 via the asynchronous boundary.

7. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman et al. U.S. 6,546,451 B1, MacWilliams et al. U.S. Patent 6,112,016 and Powell U.S. Patent 5,875,338 as applied to claim 1 above, and further in view of Chou et al. U.S. Patent 6,763,418.

Regarding claim 24, Venkataraman et al. does not teach a build-in-self-test (BIST) module as set forth in the claim. Chou et al. discloses in figures 2A and 2B a datapath 20 includes crossbar 22 to which eight communication ports 24 are coupled. Figure 2A shows an arbiter 36. In addition of eight communication ports 24, a management port 26 and a functional BIST port 28 are also coupled to crossbar 22; see figure 2B. Venkataraman et al. and Chou et al. teachings are in the same field of endeavor. Chou et al. invention differs from Venkataraman et al. invention in that Chou et al. teachings include a functional BIST port. In light of Chou et al. teachings, it would have been obvious for one of ordinary skill in the art at the time the invention was made that Venkataraman et al. crossbar unit can be modified to include a BIST as taught by Chou et al.. The modification is obvious because the BIST can be used for testing data transmission between the interfaces through crossbar unit.

8. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman et al. U.S. 6,546,451 B1, MacWilliams et al. U.S. Patent 6,112,016 and Powell U.S. Patent 5,875,338 as applied to claim 1 above, and further in view of Barber et al. U.S. Patent 4,849,751.

Regarding claim 31, Venkataraman et al. does not teach the node controller 12 including crossbar switch is implemented on a CMOS integrated circuit as set forth in the application claim. Barber et al., nevertheless, teaches a CMOS integrated circuit digital crossbar switching arrangement shown in figure 5 of another US Patent. CMOS technology is mature and well known in the art. Because of the known benefits of CMOS technology, one of ordinary skill in the art at the time the invention was made would have been motivated to implement Venkataraman et al. node controller 12 including crossbar unit on a CMOS integrated circuit as taught in Barber et al. invention.

9. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman et al. U.S. 6,546,451 B1, MacWilliams et al. U.S. Patent 6,112,016 and Powell U.S. Patent 5,875,338 as applied to claim 1 above, and further in view of Ristau et al. U.S. Patent 6,374,307 B1.

Regarding claim 27, Venkataraman et al. does not teach the integrated circuit comprises a synchronous optical network (SONET) interconnect switch, the plurality of synchronous modules comprising a plurality of SONET interfaces as claimed in the application claim. Nevertheless, Ristau et al. teaches application of crossbar switch in an optical networks system in another US Patent. In column 7, lines 35-67, Ristau et al.

teaches the billing/pin register 120 in figure 1 includes a CISCO 12000 gigabit switch router (GSR). CISCO GSR line cards are designed for transmission of IP-packets or asynchronous transmission mode (ATM) cells over SONET-based optical interfaces at wire speed. *At the heart of the GSR is a multi-gigabit crossbar switching fabric.* In light of Ristau et al. teachings, it would have been obvious for one of ordinary skill in the art at the time the invention was made that the concept of applying crossbar switch, which is taught in Venkataraman et al. invention, to SONET-based optical interfaces can be realized and implemented as taught in Ristau et al. invention. The motivation is shown in Ristau et al. teachings recited above. Further teachings expresses that CISCO GSR line cards are designed for transmission of IP-packets or asynchronous transmission mode (ATM) cells over SONET-based optical interfaces at wire speed and are exchangeable across all GSR models. CISCO 12000 gigabit switch router (GSR) corresponds to the claimed synchronous optical network (SONET) interconnect switch. Furthermore, implementation of new intended use (e.g. SONET interconnect switch) for an old product does not make a claim to that old product patentable. In re Schreiber, 44 USPQ2d (Fed. Cir. 1997).

10. Claims 32-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkataraman et al. U.S. 6,546,451 B1, MacWilliams et al. U.S. Patent 6,112,016 and Powell U.S. Patent 5,875,338 as applied to claim 1 above, and further in view of Butts et al. U.S. Patent 6,002,861.

Regarding claim 32, Venkataraman et al. does not teach a computer-readable medium having data structures stored representative of the computer-bus switch architecture. However, as well known in the art of digital logic network design, one performs simulation of functional circuit design before actually building the digital logic network permanently. Butts et al. discusses such simulation in another US patent, wherein a method is disclosed for performing simulation of functional circuit design using a hardware and software emulation system. As disclosed in the abstract, Butts et al. teachings utilize a plurality of electronically reconfigurable gate array logic chips interconnected via a reconfigurable interconnect, which comprises a partial crossbar. The reconfigurable interconnect permits the digital network realized on the interconnected chips to be changed at will. Since Butts et al. teachings are in the same field of endeavor, and utilizes same components (e.g. logic chips, reconfigurable crossbar, ...) to simulate a digital network in the design, one of ordinary skill in the art would have been motivated to implement computer instructions stored a computer readable medium as data structures to simulate Venkataraman et al. teachings, as part of the preliminary design before actually building it.

Regarding claim 33, said claim is rejected on the same ground as for claim 32 because the claimed simulatable representation is discussed in claim 32.

Regarding claim 34, figure 43 in Butts et al. invention illustrates a block diagram of a Realizer design conversion system including netlists for logic chips. The Realizer

design conversion system is part of hardware and software emulation system taught in Butts et al. invention.

Regarding claim 35, as recited in claim 32, Butts et al. discloses a method for performing simulation of a digital logic network as part of design using a hardware and software emulation system. In view of that, one of ordinary skill in the art would have recognized that the data structures as part of the hardware and software emulation system can be implemented to include code description representative of Venkataraman et al. teachings.

Regarding claim 36, using analogous argument as for claim 35, the code description would correspond to a hardware description language as part of the hardware and software emulation system.

Regarding claim 37, as discussed in claim 32, since Butts et al. teachings utilize a plurality of electronically reconfigurable gate array logic chips interconnected via a reconfigurable crossbar, corresponding to the claimed set of semiconductor processing masks, it would have been obvious for one of ordinary skill in the art that the logic chips and reconfigurable crossbar as taught by Butts et al. can be implemented to represent at least a portion of Venkataraman et al. teachings.

Allowable Subject Matter

11. Claims 2-10, 14, 16-17, 25-26, 28, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shinohara U.S. Patent 6,721,324 B1 discloses "Switch Control System In ATM Switching System".

Benayoun et al. U.S. 2002/0034185 A1 discloses "System For Transmitting Local Area Network (LAN) Data Frames".

Benayoun et al. U.S. 2002/0021694 A1 discloses "System For Transmitting Local Area Network (LAN) Data Frames Through An Asynchronous Transfer Mode (ATM) Crossbar Switch".

Du U.S. Patent 6,324,180 B1 discloses "Asynchronous Transfer Mode Local Area Network Having A Ring Structure With Wireless Terminals".

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh cong Tran 02/02/2005
Examiner KHANH TRAN